In the Claims:

1-6. (cancelled)

7. (new) An integrated circuit comprising:

A. a substrate of semiconductor material;

B. functional circuitry formed on the substrate, the functional circuitry including functional registers providing stimulus outputs to the functional circuitry and response inputs from the functional circuitry;

C. at least two serial scan paths formed of the functional registers, each scan path having a serial scan input and a serial scan output;

D. at least two output devices formed on the substrate, each output device having a data input connected to the serial scan output of one scan path and having a data output with the data outputs of both output devices being connected together, each output device having a control input for selectively connecting a data signal at its data input to its data output; and

E. scan path control circuitry formed on the substrate, the control circuitry having at least two separate control output leads, each control output lead being connected to one of the scan paths and to the control input of the output device connected to that scan path, the scan path control circuit including a state machine, the state machine having state circuitry providing:

i. an Idle state;

ii. a Capture state; and

iii. at least a first Shift state and a second Shift state, there being only one Shift state for each scan path.

8. (new) The circuit of claim 7 in which the functional circuitry has a functional mode and a test mode, and the

state circuitry provides the Idle state in response to the functional circuitry being in the functional mode.

9. (new) The circuit of claim 7 in which the functional circuitry has a functional mode and a test mode, and the state circuitry transitions from the Idle state to the Capture state in response to the functional circuitry transitioning from the functional mode to the test mode.

10. (new) The circuit of claim 7 in which the state circuitry in the Capture state outputs control signals on all control output leads for the functional registers in all scan paths to capture response data from the functional circuitry.

11. (new) The circuit of claim 7 in which the state circuitry transitions from the Capture state to the first Shift state and from the first Shift state to the second Shift state.

12. (new) The circuit of claim 7 in which the state circuitry in the first Shift state outputs control signals on one control output lead selectively to connect the output of one scan path to the data output of one output device, and in which the state circuitry in the first Shift state outputs control signals on the other control output lead selectively to disconnect the output of the other scan path from the data output of the other output device.

13. (new) The circuit of claim 12 in which the state circuitry in the second Shift state outputs control signals on the one control output lead selectively to disconnect the output of the one scan path from the data output of the one output device, and in which the state circuitry in the second Shift state outputs control signals on the other control output lead selectively to connect the output of the

other scan path to the data output of the other output device.

14. (new) The circuit of claim 7 in which the serial scan inputs of all the scan paths are connected to one another.

15. (new) The circuit of claim 7 in which the functional circuitry is combinational circuitry.